

REMARKS

This is a re-submission in response to a notice of a non-compliant amendment dated April 15, 2005. In the Office Action of January 14, 2005, made final, the Examiner objected to claims 1-7 for an informality in claim 1, rejected claims 9-13 under 35 U.S.C. 112, second paragraph as being indefinite, and rejected claims 1-18 under 35 U.S.C. 103 as being obvious. Claims 1-18 remain in the application.

The informality of claim 1 was for repeating a word. This has been addressed by amending claim 1.

The rejection for indefiniteness was specifically for errors in claims 9, 10, and 13. These three claims have been amended accordingly.

The Examiner largely reiterated the previous reasoning for the obviousness rejections and then concluded with two paragraphs that addressed applicants' response. Applicants accordingly also provide applicants' previous arguments and also a response to the Examiner's position with regard to applicants' previous response using the same order as the Examiner.

The Examiner's rejection for obviousness used Child as the primary reference. Child discloses a circuit that performs a single type of hash function (SHA) serially instead of applicants' parallel approach that can also selectively perform more than one type of hash function. Applicants' approach is both faster and requires less space on the integrated circuit.

With regard to claim 1, the Examiner used Childs and four additional references, Ober, Schneier, Turner, and Batchner, to come to conclusion that claim 1 was obvious to one of ordinary skill in the art. The claimed first multiplexer is useful in allowing for the use of the register file for both hash modes. The Examiner states that this claimed first multiplexer is obvious because multiplexers are known to switch between a signal and a reference and that this claimed location in the circuit is obvious because there is an incentive to minimize the number of elements. In effect the Examiner is saying two things: (1) one of ordinary skill in the art would recognize the benefit of applicants' invention and (2) anytime known elements are used to achieve a benefit that is recognizable to one of ordinary skill in the art, it is obvious for one of ordinary skill in the art to have done so. Applicants agree with the first but not the second. The Examiner's application of the legal requirement for an incentive to combine implies that anytime a circuit that uses transistors of the type known in the art for switching or amplification and such circuit provides a known desired benefit such as reducing circuit elements or improving speed,

such circuit is obvious and unpatentable. In this case there is no suggestion in the prior art that the elements that are combined by Applicants can be combined in the manner claimed by Applicants. Ober teaches that both hash functions can exist on the same integrated circuit, but applicants have not been able to find any reference that there is any suggestion that these two functions can share the same circuitry much less teach which elements can be shared. The Examiner is applying hindsight using Applicants' teaching to construct from the prior art the resulting claimed circuits. Accordingly, applicants submit that claim 1 patentably distinguishes over the five reference combination applied by the Examiner.

With regard to claims 2-7, the Examiner continued to apply the same approach that because Applicants used known circuit elements in achieving the result and the result was beneficial, the result was obvious. Applicants disagree as stated above.

Independent claim 8 claims an adder with a first, second, third, fourth, and fifth input. Childs discloses a two input adder 522. Notice that applicants' circuit does not require multiplexer 501 and flip-flops 502-506. Childs needs these flip-flops as temporary storage for chaining variables. This makes the operation significantly slower. Further, these flip-flops require more space than the additional space required over a two input adder. Also multiplexer 520 is not required and accumulator 523 is not used. There are multiplexers used to control the inputs to the five input adder, but these are for the different modes, SHA-1 and MD5. Once the mode is selected these multiplexers simply feedthrough the input for that mode. There is no switching between inputs to the adder during the determination of the hash output. In Childs, multiplexers 521 and 520 are switching inputs (serial approach) to adder 522 during the determination of the hash output, thus being significantly slower in determining the hash output than applicants' five input adder (parallel approach) manner of performing the hash function. Accordingly, applicants submit that claim 8 is patentably distinct from the art cited by the Examiner.

With regard to claims 9-13, the Examiner continued to apply the same approach used against claim 1 that because Applicants used known circuit elements in achieving the result and the result was beneficial, the result was obvious. Applicants disagree as stated above.

With regard to independent claim 14 and dependent claims 15-18, the Examiner used the same type of argument used in against claim 1. Applicants disagree with this reasoning as per the response for claim 1.

With regard to claim 15, Applicants submit that element 603 of Childs is not a decoder and thus is not appropriate as being asserted as being analogous to the claimed decoder of claim 15.

Further with regard to claim 16 as amended, the analogy used by the Examiner is not a correct representation of the prior art. The Exclusive Or claimed is not analogous to that of Childs 605.

With regard to the Examiner's new portions of the response, the analysis of claim 8 was altered but still used the same approach used previously and used in rejecting other claims. The Examiner's view of his analysis regarding all of the claims is that hindsight engineering is ok so long as it is not only taught by applicants and cited *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this regard, most of the claimed connections are only taught by applicants so the Examiner's view of that holding does not help the Examiner's case. The Examiner's approach has been to start with applicants' invention and the advantage thereof and see if the various claim elements exist in the prior art and see if one ordinary skill in the art would have been able to use the prior the art to achieve applicants invention after having seen applicants invention and would understand there is a benefit. Under this test it's difficult to imagine that there is any circuit that uses only known elements such as transistors, resistors, and capacitors that would be patentable. The proper test is that the prior art itself must provide the motivation to combine not that one of ordinary skill in the art would be able to build applicants' invention and appreciate its benefits after having been taught applicants' invention. Accordingly, applicants submit that the rejection of claims 1-18 is improper because of the improper analysis of the Examiner.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

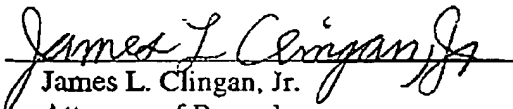
Applicants believe the application is in condition for allowance which action is respectfully solicited. Please contact the below-signed if there are any issues regarding this communication or otherwise concerning the current application.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
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FEE TRANSMITTAL		Complete if Known	
Patent fees are subject to annual revision <input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27		Application Number	09/725,821
		Filing Date	November 29, 2000
		First Named Inventor	James D. Dworkin et al
		Examiner Name	Matthew T. Henning
		Group Art Unit	2131
TOTAL AMOUNT OF PAYMENT		Attorney Docket No.	SC11015ZC
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METHOD OF PAYMENT (check all that apply)		FEE CALCULATION (continued)																																																																																																																																																											
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FEE TRANSMITTAL Patent fees are subject to annual revision <input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27		Complete if Known	
		Application Number	09/725,821
		Filing Date	November 29, 2000
		First Named Inventor	James D. Dworkin et al
		Examiner Name	Matthew T. Henning
		Group Art Unit	2131
TOTAL AMOUNT OF PAYMENT		(\$)	120
		Attorney Docket No.	SC11015ZC

METHOD OF PAYMENT (check all that apply)		FEE CALCULATION (continued)																																																																																																																																																											
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ADDITIONAL FEES <table border="1" style="width:100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2">Large Entity</th> <th colspan="2">Small Entity</th> <th rowspan="2">Fee Description</th> </tr> <tr> <th>Fee Code</th> <th>Fee (\$)</th> <th>Fee Code</th> <th>Fee (\$)</th> </tr> </thead> <tbody> <tr><td>1051</td><td>130</td><td>2051</td><td>65</td><td>Surcharge - late filing fee or oath</td></tr> <tr><td>1052</td><td>50</td><td>2052</td><td>25</td><td>Surcharge - late Provisional filing</td></tr> <tr><td>1053</td><td>130</td><td>1053</td><td>130</td><td>Non-English specification</td></tr> <tr><td>1812</td><td>2520</td><td>1812</td><td>2520</td><td>For filing a request for ex parte Reexamination</td></tr> <tr><td>1804</td><td>920*</td><td>1804</td><td>920*</td><td>Requesting publication of SIF prior to Examiner action</td></tr> <tr><td>1805</td><td>1840*</td><td>1805</td><td>1840*</td><td>Requesting publication of SIF after Examiner action</td></tr> <tr><td>1251</td><td>120</td><td>2251</td><td>55</td><td>Extension for reply within first month</td></tr> <tr><td>1252</td><td>450</td><td>2252</td><td>215</td><td>Extension for reply within second month</td></tr> <tr><td>1253</td><td>1020</td><td>2253</td><td>490</td><td>Extension for reply within third month</td></tr> <tr><td>1254</td><td>1590</td><td>2254</td><td>765</td><td>Extension for reply within fourth month</td></tr> <tr><td>1255</td><td>2160</td><td>2255</td><td>1040</td><td>Extension for reply within fifth month</td></tr> <tr><td>1401</td><td>500</td><td>2401</td><td>170</td><td>Notice of Appeal</td></tr> <tr><td>1402</td><td>500</td><td>2402</td><td>170</td><td>Filing a brief in support of an appeal</td></tr> <tr><td>1403</td><td>1000</td><td>2403</td><td>160</td><td>Request for oral hearing</td></tr> <tr><td>1451</td><td>1510</td><td>1451</td><td>1610</td><td>Petition to institute a public use proceeding</td></tr> <tr><td>1452</td><td>500</td><td>2452</td><td>55</td><td>Petition to revive - unavoidable</td></tr> <tr><td>1453</td><td>1500</td><td>2453</td><td>685</td><td>Petition to revive - unintentional</td></tr> <tr><td>1501</td><td>1400</td><td>2501</td><td>685</td><td>Utility issue fee (or reissue)</td></tr> <tr><td>1502</td><td>490</td><td>2502</td><td>245</td><td>Design issue fee</td></tr> <tr><td>1503</td><td>660</td><td>2503</td><td>330</td><td>Plant issue fee</td></tr> <tr><td>1460</td><td>130</td><td>1460</td><td>130</td><td>Petitions to the Commissioner</td></tr> <tr><td>1807</td><td>50</td><td>1807</td><td>50</td><td>Processing fee under 37 CFR 1.17(c)</td></tr> <tr><td>1808</td><td>180</td><td>1808</td><td>180</td><td>Submission of IDS</td></tr> <tr><td>8021</td><td>40</td><td>8021</td><td>40</td><td>Recording each patent assignment per property (times number of properties)</td></tr> <tr><td>1809</td><td>790</td><td>2809</td><td>395</td><td>Filing a submission after final rejection (37 CFR § 1.129(a))</td></tr> <tr><td>1810</td><td>790</td><td>2810</td><td>395</td><td>For each additional invention to be examined (37 CFR § 1.129(b))</td></tr> <tr><td>Large Fee</td><td>790</td><td>2601</td><td>395</td><td>Request for Continued Examination</td></tr> <tr><td>1802</td><td>900</td><td>1802</td><td>900</td><td>Request for expedited examination of a design application</td></tr> <tr><td colspan="5">Other fee (specify) _____</td></tr> </tbody> </table>		Large Entity		Small Entity		Fee Description	Fee Code	Fee (\$)	Fee Code	Fee (\$)	1051	130	2051	65	Surcharge - late filing fee or oath	1052	50	2052	25	Surcharge - late Provisional filing	1053	130	1053	130	Non-English specification	1812	2520	1812	2520	For filing a request for ex parte Reexamination	1804	920*	1804	920*	Requesting publication of SIF prior to Examiner action	1805	1840*	1805	1840*	Requesting publication of SIF after Examiner action	1251	120	2251	55	Extension for reply within first month	1252	450	2252	215	Extension for reply within second month	1253	1020	2253	490	Extension for reply within third month	1254	1590	2254	765	Extension for reply within fourth month	1255	2160	2255	1040	Extension for reply within fifth month	1401	500	2401	170	Notice of Appeal	1402	500	2402	170	Filing a brief in support of an appeal	1403	1000	2403	160	Request for oral hearing	1451	1510	1451	1610	Petition to institute a public use proceeding	1452	500	2452	55	Petition to revive - unavoidable	1453	1500	2453	685	Petition to revive - unintentional	1501	1400	2501	685	Utility issue fee (or reissue)	1502	490	2502	245	Design issue fee	1503	660	2503	330	Plant issue fee	1460	130	1460	130	Petitions to the Commissioner	1807	50	1807	50	Processing fee under 37 CFR 1.17(c)	1808	180	1808	180	Submission of IDS	8021	40	8021	40	Recording each patent assignment per property (times number of properties)	1809	790	2809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	Large Fee	790	2601	395	Request for Continued Examination	1802	900	1802	900	Request for expedited examination of a design application	Other fee (specify) _____				
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SUBMITTED BY		Complete (if applicable)	
Name (Print/Type)	James L. Clingan, Jr.	Registration No.	30,163
Signature	<i>James L. Clingan, Jr.</i>	Telephone	(512) 996-6338
		Date	4/28/05